Shubhani

shubhani@cse.iitd.ac.in

EDUCATION

Doctor of Philosophy *July 2016 – Present*
Department of Computer Science and Engineering Overall CGPA: 9.95/10
Indian Institute of Technology Delhi

Bachelor of Technology *2005 – 2009*
Department of Electronics and Communication Engineering Overall CGPA: 9.82/10
National Institute of Technology, Kurukshetra

PROFESSIONAL EXPERIENCE

Lead Engineer April 2014 - August 2016 **Samsung R&D Institute, New Delhi**

- RTL and Testbench development of the Display and Audio Modules.
- Development of Display and Audio modules Firmware for Arm Based STM32 microcontroller.
- FPGA Prototyping, Synthesis and Static timing analysis.
- Hardware/Software Co-Simulation.

Senior Engineer July 2009 - March 2014 **Bharat Electronics Limited, Ghaziabad**

- Performed the full hardware/software development process with the end result of deploying a large scale secure communication system that provides IPSec and Firewall over 10G ethernet network.
- Implementation of indigenously designed Proprietary Key Scheduling & Crypto algorithms in FPGA for various communication equipment.
- Design of Novel & Proprietary Metastability based TRNG for random number generation and its further optimization for passing all the statistical tests.
- Presented demonstrations and full system deployment to Defense derived clients.

RESEARCH INTERESTS

Compilers, Operating systems

PUBLICATIONS

- Shubhani Gupta, Aseem Saxena, Anmol Mahajan, and Sorav Bansal. **"Effective Use of SMT Solvers for Program Equivalence Checking Through Invariant-Sketching and Query-Decomposition"**. In Theory and Applications of Satisfiability Testing (SAT 2018). URL: https://doi.org/10.1007/978-3-319-94144-8_22
- N. Jindal, S. Gupta, D. P. Ravipati, P. R. Panda and S. R. Sarangi, **"Enhancing Network-on-Chip Performance by Reusing Trace Buffers,"** in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 39, no. 4, pp. 922-935 (April 2020) doi: 10.1109/TCAD.2019.2907909.
- Shubhani Gupta, Abhishek Rose, and Sorav Bansal. **"Counterexample-Guided Correlation Algorithm for Translation Validation"**. In: Proc. ACM Program. Lang. 4.OOPSLA (Nov. 2020). URL:https://doi.org/10.1145/3428289.

ACHIEVEMENTS

- **All India Rank 29** in National Talent Search Exam Scholarship awarded by Govt. of India 2002
- Awarded Kalpana Chawla Scholarship for **1st AIEEE Rank** among girls in Haryana 2005
- Shortlisted for O. P. Jindal Scholarship twice and have been declared as **OPJEMS'08** 2008
- Awarded with **Gold Medal** in college for best academic performance (ECE) 2005-2009
- Awarded with **highest Performance Related Pay** for all the 4 years of service in BEL 2009-2013
- Awarded with **Employee of The Quarter** for good contribution in Project in Samsung Delhi. 2015